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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,254	06/26/2003	Talal K. Jaber	42P15218	7766

8791 7590 12/28/2005

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,254	JABER ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *18-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to AMENDMENT filed 10/28/2005. Claims 1-31 are pending and presently under examination.

Objection to the Drawings under 37 CFR 1.83(a) has been withdrawn, for failing to show the "audio device" of the invention specified in the claims, in view of the amendment to the claims.

Objection to the Specification has been withdrawn in view of Applicant's arguments.

Response to Arguments

Applicant's arguments, see AMENDMENT filed 10/28/2005, with respect to the rejection of claims 1-31 under 35 U.S.C. 102(b) as being anticipated by Jaber (U.S. Patent No. 6,028,983), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made for claims 1-31, as anticipated by Nakamura (U.S. Patent No. 5,627,841) issued: May 6, 1997.

Applicant's arguments with respect to claims 1-31 are moot in view of the new ground of rejection, as set forth in the present Office Action, next.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "audio device"

recited in claim 18 on line 4, as currently amended, must be shown or the feature canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 18-25 are objected to because of the following informalities:

Claim 18, line 4, recite an "audio device", which is not shown in the drawings. Claims 19-25 are also objected because they depend from an objected claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (U.S. Patent No. 5,627,841) issued: May 6, 1997.

Regarding independent Claim 1, Nakamura discloses an apparatus for an integrated logic circuit with partial scan path circuit and partial scan path design method, Figures 2 and 3, the apparatus comprising:

First control means (operation mode control circuit 70) for controlling a signal state at each clock source (1, 2, 3) to control an operation mode of each FF, by routing a functional clock (user clock) to a functional unit in an integrated logic circuit including a combinational logic and a plurality of FFs coupled therewith and supplied with a plurality of clock signals (clocks C1, C2 and C3). The operation mode control circuit 70 comprises a supply circuit 71 of a scan sample signal and a three clock controllers (SCD) 11, 12 and 13 for responding to the scan sample signal to have a clock signal state (e.g. "1") set at each clock source (1, 2, 3), See Summary of the Invention and Figures 2 and 3.

Second control means (scan clock supply circuit 60) for supplying each scan FF 22, 23,24 with a pair of scan clocks SCLK1 and SCLK 2 for scan actions. The scan clock supply circuit 60 comprises a supply circuit 61 of the scan clock SCLK1 for a latching action to hold or sample a data, and a supply circuit 62 of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claim 2, Nakamura discloses second control means comprises (scan test circuitry) coupled to a scan path 80 as a shift register for responding to the clock source signal state and the scan clocks SCLK1 and SCLK2 to sequentially shift a scan FF test data, such as a serial pattern of functional test data.

Regarding Claim 3, Nakamura discloses a plurality of FUBs, such as functional circuit composed of a set of various logic circuits (hereafter "combinational logic") provided with a plurality of functional inputs and a plurality of functional outputs, the six FFs 1-6 coupled with the combinational logic so that various combinational logic paths and sequential data paths are established as shown by directional dashed lines, and a clock distribution system shown by directional solid lines, Figure 2.

Regarding Claims 4, 5, Nakamura discloses scan clock supply circuit 60 comprises a master clock generation circuit (supply circuit 61) of the scan clock SCLK1 for a latching action to hold or sample a data, and a slave clock generation circuit (supply circuit 62) of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claims 6, 7, Nakamura discloses wherein the first control means is a hierarchy of functional clocks (clocks C1, C2 and C3) to control the functional unit (combinational logic) during normal operation, and wherein the second control means is a hierarchy of functional clocks (SCLK1 and SCLK 2) to control the functional unit during testing.

Regarding independent Claim 8, Nakamura discloses a processor, such as a scan test circuitry, for an integrated logic circuit with partial scan path circuit and partial scan path design method, Figures 2 and 3, the processor comprising:

A functional clock hierarchy (operation mode control circuit 70) for controlling a signal state at each clock source (1, 2, 3) to control an operation mode of each FF, by routing a functional clock (user clock) to a functional unit in an integrated logic circuit including a combinational logic and a plurality of FFs coupled therewith and supplied with a plurality of clock signals (clocks C1, C2 and C3). The operation mode control circuit 70 comprises a supply circuit 71 of a scan sample signal and a three clock controllers (SCD) 11, 12 and 13 for responding to the scan sample signal to have a clock signal state (e.g. "1") set at each clock source (1, 2, 3), See Summary of the Invention and Figures 2 and 3.

A scan clock hierarchy (scan clock supply circuit 60) for supplying each scan FF 22, 23,24 with a pair of scan clocks SCLK1 and SCLK 2 for scan actions. The scan clock supply circuit 60 comprises a supply circuit 61 of the scan clock SCLK1 for a latching action to hold or sample a data, and a supply circuit 62 of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claims 9, 10, Nakamura discloses second control means comprises (scan test circuitry) coupled to a scan path 80 as a shift register for responding to the

clock source signal state and the scan clocks SCLK1 and SCLK2 to sequentially shift a scan FF test data, such as a serial pattern of functional test data.

Regarding Claims 11-13, Nakamura discloses a plurality of FUBs, such as functional circuit composed of a set of various logic circuits (hereafter "combinational logic") provided with a plurality of functional inputs and a plurality of functional outputs, the six FFs 1-6 coupled with the combinational logic so that various combinational logic paths and sequential data paths are established as shown by directional dashed lines, and a clock distribution system shown by directional solid lines, Figure 2.

Regarding Claims 14, 15, Nakamura discloses scan clock supply circuit 60 comprises a master clock generation circuit (supply circuit 61) of the scan clock SCLK1 for a latching action to hold or sample a data, and a slave clock generation circuit (supply circuit 62) of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claims 16, 17, Nakamura discloses wherein the first control means is a hierarchy of functional clocks (clocks C1, C2 and C3) to control the functional unit (combinational logic) during normal operation, and wherein the second control means is a hierarchy of functional clocks (SCLK1 and SCLK 2) to control the functional unit during testing.

Regarding independent Claim 18, Nakamura discloses a system for an integrated logic circuit with partial scan path circuit and partial scan path design method, Figures 2 and 3, the system comprising:

A scan test circuitry, including scan memory elements such as FFs. Also at step S34, data on the scan flags f1 and f2 of the FF with the current id n are output to be stored in a memory, Figure 9.

First control means (operation mode control circuit 70) for controlling a signal state at each clock source (1, 2, 3) to control an operation mode of each FF, by routing a functional clock (user clock) to a functional unit in an integrated logic circuit including a combinational logic and a plurality of FFs coupled therewith and supplied with a plurality of clock signals (clocks C1, C2 and C3). The operation mode control circuit 70 comprises a supply circuit 71 of a scan sample signal and a three clock controllers (SCD) 11, 12 and 13 for responding to the scan sample signal to have a clock signal state (e.g. "1") set at each clock source (1, 2, 3), See Summary of the Invention and Figures 2 and 3.

Second control means (scan clock supply circuit 60) for supplying each scan FF 22, 23,24 with a pair of scan clocks SCLK1 and SCLK 2 for scan actions. The scan clock supply circuit 60 comprises a supply circuit 61 of the scan clock SCLK1 for a latching action to hold or sample a data, and a supply circuit 62 of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claims 19-21, Nakamura discloses (scan clock supply circuit 60) for supplying each scan FF 22, 23,24 with a pair of scan clocks SCLK1 and SCLK 2 for scan actions. The scan clock supply circuit 60 comprises a supply circuit 61 of the scan clock SCLK1 for a latching action to hold or sample a data, and a supply circuit 62 of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Regarding Claims 22-24, Nakamura discloses a plurality of inputs and outputs of the scan FFs, using the scan clocks SCLK1 and SCLK2 to operate the scan FFs as a shift register, for inputting the test input data (SCAN IN) and outputting the test output data (SCAN OUT)

Regarding Claim 25, Nakamura discloses scan clock (SCLK1 and SCLK2) is able to operated at a slower speed than the functional clock (clocks C1, C2 and C3) without either incurring a delay, since they are both independent of each other. Providing a partial scan path design method for an integrated logic circuit cooperatively functionable even with a multiclock system or with a gated clock system, permitting an increased operation speed and a reduced chip area, see Summary of the Invention.

Regarding independent Claim 26, Nakamura discloses an apparatus for an integrated logic circuit with partial scan path circuit and partial scan path design method, Figures 2 and 3, the apparatus comprising:

First control means (operation mode control circuit 70) for controlling a signal state at each clock source (1, 2, 3) to control an operation mode of each FF, by routing a functional clock (user clock) to a functional unit in an integrated logic circuit including a combinational logic and a plurality of FFs coupled therewith and supplied with a plurality of clock signals (clocks C1, C2 and C3). The operation mode control circuit 70 comprises a supply circuit 71 of a scan sample signal and a three clock controllers (SCD) 11, 12 and 13 for responding to the scan sample signal to have a clock signal state (e.g. "1") set at each clock source (1, 2, 3), See Summary of the Invention and Figures 2 and 3.

Second control means (scan clock supply circuit 60) for supplying each scan FF 22, 23,24 with a pair of scan clocks SCLK1 and SCLK 2 for scan actions. The scan clock supply circuit 60 comprises a supply circuit 61 of the scan clock SCLK1 for a latching action to hold or sample a data, and a supply circuit 62 of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

(Scan test circuitry) coupled to a scan path 80 as a shift register for responding to the clock source signal state and the scan clocks SCLK1 and SCLK2 to sequentially shift a scan FF test data, such as a serial pattern of functional test data.

Regarding Claims 27-29, Nakamura discloses wherein the first control means is a hierarchy of functional clocks (clocks C1, C2 and C3) to control the functional unit (combinational logic) during normal operation, and wherein the second control means

is a hierarchy of functional clocks (SCLK1 and SCLK 2) to control the functional unit during testing.

Regarding Claims 30, 31, Nakamura discloses scan clock supply circuit 60 comprises a master clock generation circuit (supply circuit 61) of the scan clock SCLK1 for a latching action to hold or sample a data, and a slave clock generation circuit (supply circuit 62) of the scan clock SCLK2 for a transfer action to output the data, where the (operation mode control circuit 70) and the (scan clock supply circuit 60) are independent of each other, See Summary of the Invention and Figures 2 and 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: _____

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Date: 19 December 2005
Office Action: Non-Final Rejection